said semiconductor element to an external circuit of said semiconductor element;

an insulating film having an opening portion configured to accommodate said semiconductor element and to support said plurality of lead wires connected to the plurality of connecting electrodes of the semiconductor element and said at least the single dummy lead wire; and

a resin molding configured to cover a connecting portion between tip portions of the plurality of lead wires and the plurality of connecting electrodes and a tip portion of said at least the single dummy lead wire within the opening portion of said insulating film,

wherein said at least a single dummy lead wire is arranged in a space defined by two adjacent lead wires of said plurality of lead wires so that a length of said space is at least twice a minimum pitch between adjacent lead wires of said plurality of lead wires,

wherein the tip portion of said at least the single dummy lead wire covered with said resin molding is positioned between a peripheral portion of said opening portion and a peripheral portion of the semiconductor element arranged within the opening portion, and

wherein at least two adjacent dummy lead wires are arranged on said semiconductor device and tip portions of the at least two adjacent dummy lead wires, which have no lead wires therebetween, are connected to each other.

29. (New) A semiconductor memory device comprising:

a semiconductor element;

a plurality of lead wires connected to a plurality of connecting electrodes formed on said semiconductor element;

at least a single dummy lead wire that is not electrically connected to said semiconductor element and does not include an outer lead portion for electrically connecting said semiconductor element to an external circuit of said semiconductor element;

an insulating film having an opening portion configured to accommodate said semiconductor element and to support said plurality of lead wires connected to the plurality of connecting electrodes of the semiconductor element and said at least the single dummy lead wire; and

a resin molding configured to cover a connecting portion between tip portions of the plurality of lead wires and the plurality of connecting electrodes and a tip portion of said at least the single dummy lead wire within the opening of said insulating film,

wherein said at least a single dummy lead wire is arranged in a space defined by two adjacent lead wires of said plurality of lead wires so that a length of said space is at least twice a minimum pitch between adjacent lead wires of said plurality of lead wires, and

wherein a dummy lead wire is formed on each of two opposing sides of said semiconductor element and tip portions of the dummy lead wires positioned to face each other are connected to each other to form a straight single dummy lead wire.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

This application is a Request for Continued Examination (RCE) of application S/N 09/740,902, filed on December 21, 2000. This amendment is similar to the previous amendment, which was not entered.

Claims 28 and 29 are pending in the present application. Claims 1-3, 5, 6, 9, 11 and 13 have been cancelled and Claims 28 and 29 have been added by the present amendment.

In the outstanding Office Action, Claims 1-3 and 13 were rejected under 35 U.S.C. § 102(b) as anticipated by Oshino et al; Claims 5, 9 and 11 were rejected under 35 U.S.C.

§ 103(a) as unpatentable over Oshino et al in view of Lamson et al; and Claim 6 was rejected under 35 U.S.C. § 103(a) as unpatentable over Oshino et al in view of Hartman.

All rejected claims have been cancelled. New Claims 28 and 29 include features of Claims 1, 2 and 9 and of Claims 1 and 6, respectively. Claims 28 and 29 find support in the now cancelled Claims 1, 2, 6 and 9 and in Figures 2A, 3A and 4A. No new matter has been added.

Accordingly, arguments will be presented distinguishing Claim 28 over Oshino et al and Lamson et al, and distinguishing Claim 29 over Oshino et al and Hartman.

Claim 28 is directed to a semiconductor device having at least a single dummy lead wire arranged in a space defined by two adjacent lead wires of a plurality of lead wires so that a length of the space is at least twice a minimum pitch between adjacent lead wires of the plurality of lead wires. In addition, a tip portion of at least a single dummy lead wire is positioned between a peripheral portion of an opening portion of an insulating film and a peripheral portion of a semiconductor element arranged within the opening portion. Furthermore, two adjacent dummy lead wires are arranged in the semiconductor device and a tip portion of the two adjacent dummy lead wires, which have no lead wires therebetween, are connected to each other.

In a non-limiting example, Figure 3A shows the semiconductor element 21 placed in the opening 26 of the insulating film 22 so that at least a single dummy lead wire 23' is arranged in the space between two adjacent lead wires 23 and the length of the space is at least twice the minimum pitch between adjacent lead wires 23. Further, the tip portion of at least the single dummy lead wire 23' is positioned between the peripheral portion of the opening portion 26 and the peripheral portion of the semiconductor element 21. In addition, two adjacent dummy lead wires 33", as shown in Figure 4A, are arranged so that tip portions

of the two adjacent dummy lead wires, which have no lead wires in between, are connected to each other.

An advantage of the structure recited in Claim 28 is an improved mechanical strength and a prevention of cracking between the semiconductor chip and the resin mold.[1]

Oshino et al disclose in Figure 1 a dummy lead wire 5B disposed on an insulating layer 6. However, Oshino et al do not teach or disclose at least a single dummy lead wire arranged in a space defined by two adjacent lead wires so that a length of said space is at least twice a minimum pitch between adjacent lead wires, and tip portions of two adjacent dummy lead wires which have no lead wires in between are connected to each other.

Lamson et al disclose a lead frame 10 in Figure 1 connected over an integrated circuit 14 by adhesives 42 and 44. Further, the ends of the dummy lead wires in Lamson et al extend over the IC chip and the ends of two adjacent dummy leads 32 and 34 are connected to each other. More specifically, as shown in Figure 2 of Lamson et al and as described at column 3, line 68 to column 4, line 2, the support bars 32 and 34 are provided on the double-sided adhesives 42 and 44 at both ends of the IC chip 40 to press the double-sided adhesives 42 and 44 against the chip surface. However, Lamson et al do not teach or suggest dummy lead wires with tip portions positioned between a peripheral portion of an opening portion of an insulating layer and a peripheral portion of the semiconductor element arranged within the opening portion, and tip portions of at least two adjacent dummy lead wires which have no lead wires therebetween, connected to each other.

In addition, to the contrary of the present invention, all the lead wires in Lamson et al are connected to the lead frame 10 (Figure 2) and there is not a single dummy lead wire

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[1]Specification, page 13, lines 1-8.

disposed as recited in Claim 28.

Accordingly, it is respectfully submitted independent Claim 28 patentably distinguishes over Oshino et al and Lamson et al.

Claim 29 includes features similar to those discussed in Claim 28 and further includes dummy lead wires formed on each of two opposing sides of the semiconductor element so that tip portions of the dummy lead wires are positioned to face and connect to each other to form a single dummy lead wire.

Hartman discloses a discretionary wiring on a semiconductor chip formed directly on a semiconductor substrate during a stage referred to as wafer process of the manufacturing process of semiconductor devices. More specifically, the discretionary wiring is performed using multilevel metallization formed directly on the semiconductor substrate as shown in Figures 2-5 in Hartman.

In contrast, in Claim 29 of the present invention, the tip portions of the dummy lead wire 33" are formed on the opening portion 36 of the insulating film 32 to face each other and are connected to each other to form a straight line single lead wire, as shown in Figures 4A and 4B. In more detail, Figure 4B shows the dummy lead wire 33" is not a metallization formed directly on the semiconductor chip but it is fixed to the surface of the semiconductor chip for the first time in the resin molding step that is usually included in the assembly process.

In other words, the dummy lead wire 33" recited in Claim 29, together with other lead wires or dummy lead wires, are adhered to the insulating film that serves as an interposer and then, the result of the interposer structure is transferred to the assembly process including the steps of electrically connecting the lead wires and the semiconductor chip and resin molding.

Thus, Hartman do not teach or suggest at least a single dummy lead wire arranged in a

space defined by two adjacent lead wires so that the length of the space is at least twice a minimum pitch between adjacent lead wires and a tip portion of at least a single dummy lead wire covered with the resin molding is positioned between a peripheral portion of an opening portion of an insulating film and a peripheral portion of the semiconductor element.

Accordingly, it is respectfully submitted independent Claim 29 is also allowable.

Further, it is respectfully requested this amendment be entered as it is believed no new issues have been raised.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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